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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,763	01/31/2006	Godefridus Johannes Geelen	NL03 0935 US1	6167

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER

CHENG, DIANA

ART UNIT	PAPER NUMBER
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2816

NOTIFICATION DATE	DELIVERY MODE
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11/21/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/566,763	Applicant(s) GEELEN, GODEFRIDUS JOHANNES	
	Examiner Diana J. Cheng	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,4 and 6-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4 and 6-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claim 1, 3, 4, and 6-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1, 3, 4, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570), and in view of Applicant's Admitted Prior Art (AAPA).**

Re claim 1, Dedic discloses in Fig. 1 a single track-and-hold circuit comprising: an input signal V_i , an output signal V_o , a switch 1, capacitor 2, and high-impedance unity-gain amplifier 3, where in Fig. 2, the amplifier contains a current source 32, and a buffering transistor 33, but does not teach the circuitry details of the first and second bootstrap switches.

AAPA in Fig. 3 teaches a single track-and-hold circuit having an input signal (V_{in}) and an output signal (V), a bootstrap switch (14a) having as its inputs a clock signal and an input signal (vin); said single track-and-hold circuit further comprising a capacitor ($Chold$), said input signal (V_{in}) being connected to said capacitor ($Chold$) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal ($clkboot$) equal to said input signal (V_{in}) added to a supply voltage (V_{dd}); and

including a second bootstrap switch (14b).

AAPA teaches that Fig. 3 is an improvement upon Fig. 1, which includes a switch and capacitor, and acts as a simple track-and-hold circuit. Fig. 1 of AAPA is equivalent to the switch 1 and capacitor 2 of Dedic.

Therefore, it would have been obvious to one of ordinary skill in the art to use the teachings of AAPA of a track and hold circuit, to be used in place of switch 1 and capacitor 2 of Dedic (as also described by the AAPA Fig. 1 as a simple track-and-hold circuit) for the purpose of suppressing the offset and distortion of AAPA Fig. 1.

The combined teachings of Dedic and AAPA further teach said input signal (AAPA, Fig. 3, vin) of said bootstrap switch (AAPA, Fig. 3, 14a) being connected to said output signal (Dedic, V_o) of said circuit via a current source (Dedic, 32) and a buffering transistor (Dedic, 33), characterized in that said input signal (AAPA, Fig. 3, vin) of said bootstrap switch (AAPA, Fig. 3, 14a) comprises said output signal (Dedic, V_o) of said circuit; and

the input signal (AAPA, Fig. 3, vin) of which is connected to said output signal (Dedic, Vs) of said single track-and-hold circuit via said current source (Dedic, 32) and said buffering transistor (Dedic, 33) of said single track-and-hold circuit.

Re claim 3, Dedic and AAPA, as a whole, teach single a track-and-hold circuit according to the present invention, wherein said buffering transistor (Dedic, 33) comprises a MOS transistor [Fig. 2, 33; Fig. 4, 31].

Re claim 4, Dedic and AAPA, as a whole, teach a single track-and-hold circuit according to the present invention, wherein Dedic further teaches said MOS transistor (33) is a PMOS transistor [Fig. 4, 33, 34].

Re claim 6, Dedic and AAPA, as a whole, further teach a single track and hold circuit in AAPA further comprising one or more dummy switches (16) which are clocked in anti-phase (Specification, lines 22-23) to said switch (10) connecting said input signal (Vin) to said capacitor (12).

Re claim 7, Dedic and AAPA, as a whole, teach a single track and hold circuit wherein said input signal (Vin) is connected to said dummy switches (16) via a bootstrap switch (14b), having as an additional input an anti-phase clock signal (Specification, lines 22-23).

Re claim 8, Dedic and AAPA, as a whole, teach an analog-to-digital converter including a single track-and-hold circuit according to the present invention [Dedic, Col. 1, lines 6-9].

Re claim 9, Dedic and AAPA, as a whole, teach an integrated circuit including an analog-to-digital converter according to the present invention [where it would be inherent for an analog-to-digital converter be used in an integrated circuit].

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J. Cheng whose telephone number is (571)270-1197. The examiner can normally be reached on Monday-Friday, 9 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln D. Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. J. C./
Examiner, Art Unit 2816
11/15/2008